NOTICE OF ALLOWANCE

This is a NOTICE OF ALLOWANCE in response to the AMENDMENT filed 1/6/2009.

The present US Application 10586217, filed 07/14/2006, is a national stage entry of PCT/IB05/50152 international, filed 01/13/2005.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file, for the (EPO) Patent Application No. 04100143.9, filed 01/19/2004.

The Replacement Drawings received on 8/29/2008 are acceptable

Claims 1-10 remain in the Application.

Allowable Subject Matter

Claims 1-10 are allowed.

The following is an examiner's statement of reasons for allowance:

The prior art of record taken alone or in combination fail to teach, anticipate, or render obvious a circuit testing system and method for testing a circuit under test, as recited in the independent claims 1, 3 and 6, including among other limitations, "a test pattern selector arranged to select a set of test input patterns and the associated combinations of domain clock signals, where the response to the particular test pattern captured by a timing sensitive flip-flop cell in a first clock domain is indicative of a fault condition, and where the timing sensitive flip-flop cell receives data dependent on data

from a source flip-flop cell that operates on a second clock domain different from the first clock domain".

Similarly, independent Claims 7, 9 and 10 recite a method and test pattern generating machine for generating a set of test patterns for a circuit under test, including among other limitations, "receiving information representing an original design that corresponds to the circuit under test, generating an adapted version of the original design, and selecting the set of test patterns with associated clock status signals for the adapted version so that a set of logic circuit faults is covered for the adapted version".

Consequently, Claims 1-10 are allowed over the prior arts of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JAMES C KERVEROS/
Primary Examiner, Art Unit 2117

Date: 27 February 2009
Office Action: Allowance

U.S. Patent & Trademark Office
Alexandria, VA 22314.
Tel: (571) 272-3824, Fax: (571) 273-3824
Email: james.kerveros@uspto.gov